1. A method of forming a stacked-gate flash memory having a shallow trench isolation with a high-step oxide and high lateral coupling comprising the steps of:

providing a semiconductor substrate;

forming a pad oxide layer over said substrate;

forming a high nitride layer over said pad oxide layer;

forming and patterning a first photoresist layer over said first nitride layer to define active regions in said substrate;

forming a trench in said substrate by etching through patterns in said first photoresist layer;

removing said first photoresist layer;

forming a conformal lining on the inside walls of said trench;

depositing isolation oxide inside said trench to form shallow trench isolation (STI) with a high-step oxide;

performing chemical-mechanical polishing of said substrate;

removing said nitride layer, thus forming openings between said high-steps of said STI;

removing said pad oxide layer at the bottom of said openings between said high-steps of said STI;

forming sacrificial oxide layer over said substrate;

removing said sacrificial oxide layer;

growing floating gate oxide layer over said substrate;

forming first polysilicon layer conformally filling said openings between said high-steps of said STI;

forming and patterning a second photoresist layer over said substrate to define said first polysilicon layer and form floating gate regions in said substrate;

etching said first polysilicon layer to form floating gates;

removing said second photoresist layer;

forming interpoly oxide over said floating gate;

forming a second polysilicon layer over said interpoly oxide layer;

forming and patterning a third photoresist layer over said interpoly oxide layer to define control gate and word line;

etching through said patterning in third potoresist layer to form said word line;

removing said third photoresist layer;

forming and patterning a fourth photoresist layer over said substrate to define self-aligned source (SAS) regions in said substrate;

etching said SAS regions; and

removing said fourth photoresist layer.

2. The method of claim 1, wherein said semiconductor substrate is silicon.

3. The method of claim 1, wherein said forming pad oxide
layer is accomplished by thermal growth at a temperature
3 between about 850 to 950 °C.

4. The method of claim 1, wherein said pad oxide layer has
a thickness between about 100 to 250 angstroms (Å).

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5. The method of claim 1, wherein said forming said high
nitride layer over said pad oxide layer is accomplished by
3 CVD at a temperature between about 750 to 850 °C by reacting
dichlorosilane ($SiCl_2H_2$) with ammonia (NH_3).

6. The method of claim 1, wherein the thickness of said
high nitride layer is between about 2000 to 6000 Å.

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7. The method of claim 1, wherein said first photoresist
layer has a thickness between about 0.8 to 1.0 μm.

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8. The method of claim 1, wherein said forming a trench in
said substrate by etching through patterns in said first
3 photoresist layer into said substrate is accomplished with
etch recipe comprising gases Ar, CHF_3, C_4F_8.

9. The method of claim 1, wherein said trench has a depth
between about 2500 to 5000 Å.

10. The method of claim 1, wherein said removing said first photoresist layer is accomplished by oxygen plasma ashing.

11. The method of claim 1, wherein said conformal lining comprises an oxide having a thickness between about 100 to 450 Å.

12. The method of claim 1, wherein said depositing said isolation oxide inside said trench to form shallow trench isolation (STI) with a high-step is accomplished by using LPCVD or HDP methods.

13. The method of claim 12, wherein the thickness of said high-step oxide above said trench is between about 3000 to 7000 Å which is then reduced to between about 2000 to 6000 Å through chemical-mechanical polishing.

14. The method of claim 1, wherein said removing said nitride layer forming openings between said high-steps of said STI is accomplished with an etch recipe comprising gases SF_6 and O_2.

15. The method of claim 1, wherein said removing said pad oxide layer at the bottom of said openings between said

high-steps of said STI is accomplished with a recipe comprising gases CHF_3, CF_4 and O_2.

16. The method of claim 1, wherein said forming sacrificial oxide layer over said substrate is accomplished through thermal growth.

17. The method of claim 1, wherein said removing said sacrificial oxide is accomplished with a recipe comprising gas SF_6.

18. The method of claim 1, wherein said growing floating gate oxide layer over said substrate is accomplished by thermal growth at a temperature between about 780 to 900 °C.

19. The method of claim 1, wherein said forming a first polysilicon layer is accomplished with silicon source SiH_4 using LPCVD at a temperature between about 500 to 650°C.

20. The method of claim 1, wherein said first polysilicon layer has a thickness between about 100 to 500 Å.

21. The method of claim 1, wherein said second photoresist layer has a thickness between about 1.0 to 1.2 µm.

22. The method of claim 1, wherein said etching said first polysilicon layer is accomplished with a recipe comprising Cl_2, HBr and O_2.

23. The method of claim 1, wherein said interpoly oxide layer comprises oxide/nitride/oxide (ONO) having a thickness between about 130 to 250 Å.

24. The method of claim 1, wherein said forming a second polysilicon layer is accomplished with silicon source SiH_4 using LPCVD at a temperature between about 500 to 650°C.

25. The method of claim 1, wherein said second polysilicon layer has a thickness between about 1000 to 3000 Å.

26. The method of claim 1, wherein said third photoresist layer has a thickness between about 1.0 to 1.2 Å.

27. The method of claim 1, wherein said etching through said patterning in third potoresist layer to form said word line is accomplished with a recipe comprising Cl_2, HBr, O_2 and C_2H_6.

28. The method of claim 1, wherein said etching said SAS regions is accomplished with a recipe comprising CHF_3, CF_4 and O_2.

29. A stacked-gate flash memory having a shallow trench isolation with a high-step oxide and high lateral coupling comprising:

a trench with a high-step oxide;

a conformal layer lining the inside walls of said trench;

an opening adjacent to said trench with a high-step oxide;

a first polysilicon layer conformally lining said opening including high-step oxide of said trench to form a floating gate;

an ONO layer covering said substrate including walls of said floating gate lining said opening;

a second polysilicon layer covering said ONO layer to form a control gate; and

a self-aligned source (SAS) line.

30. The stacked-gate flash memory cell of 29, wherein said trench with a high-step oxide has a depth between about 2500 to 5000 Å.

31. The stacked-gate flash memory cell of 29, wherein said high-step oxide above said trench has a height between about 2000 to 6000 Å.

32. The stacked-gate flash memory cell of 29, wherein said conformal lining layer comprises oxide having a thickness between about 2500 to 5000 Å.

33. The stacked-gate flash memory cell of 29, wherein said opening has a width between about 1500 to 5000 Å.

34. The stacked-gate flash memory cell of 29, wherein said first polysilicon layer has a thickness between about 100 to 500 Å.

35. The stacked-gate flash memory cell of 29, wherein said second polysilicon layer has a thickness between about 1000 to 3000 Å.